Jerry Twomey

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Position Desired: Electronic product design, semiconductors or medical devices. Experienced with analog, mixed signal and RF design. Have done IC, PCB, and system level design. Have been a hands-on designer, a technical lead, and managed many successful and profitable product designs.

Experience:

November 2003 – Present: **Effective Electrons,** San Diego California – Contract circuit design and OEM support services. This includes both semiconductor and medical electronics design:

Semiconductors and Systems:

- UWB receiver, 250 MHz BW, gmC filters and auto-calibration system, SiGe BiCMOS
- Radiation hardened PLL frequency synthesizer, 90nm SOI-CMOS
- SerDes transmitter/receiver, 20 GB/sec over copper, with adaptive transmitter-receivers 65nm CMOS
- ESD protection and I/O drivers, 6KV HBM, 90nm SOI-CMOS
- RF receiver signal processing (Matlab-Simulink system modeling)
- PCI Express transmitter, 45nm CMOS
- Micro-power crystal oscillator for wide process variance, 45nm CMOS
- LVDS Receiver/Transmitter, w/pre-emphasis, 90nm SOI-CMOS
- Control system for optical data receiver
- Electromagnetic simulation for RF signal paths at 6-18GHz

Medical Devices:

- Wearable EEG system and RF link to Android cell phone. (analog front end with Bluetooth SOC)
- Distributed robotics for automated laboratory sampling system. (power systems, network controls)
- Point of care medical instrument used in HIV testing. (sensors, power, motor drivers, microcontroller)
- Cardiac arrest, therapeutic hypothermia induction (sensors, feedback, microcontroller, Verilog FPGA)
- Blood glucose personal monitor (RF links, antenna polar plots, power optimization)
- Insulin IV pump controller w/blood glucose monitor (sensor signal processing, pump drivers)
- Medical, muscle motion stimulus, (strain gauge system, encoder sensors motor drivers, microcontroller)

All medical devices were IEC 60601-1 or IEC 61010 compliant designs, including failure management compliance/risk matrix, patient isolation safety design, EMC compliance (RFI, EFT, RF common mode, Magnetic fields, ESD) and functional redundancy methods.

Other Items:

- Teaching mixed signal IC design seminars
- Program management of designers for the chip set IC's used in a satellite down-converter box.

October 2002 – October 2003: **Axiom Microdevices**, Orange/Anaheim, California
CMOS RF Power Amplifiers for GSM cell phones. Series A start-up included IC design, layout, technical infrastructure, and staffing activities. This included:

- RF Front end driver circuits for PA
- PA linearity, phase noise analysis
- ESD I/O design
- PA Power management and control system
- Design team staffing, IT and EDA support
- Foundry/Process Qualification

September 2000 – August 2002: **IBM - RF Design Center,** Encinitas, California
Wireless IC Design: Development of direct conversion receivers for 3G cellular phones, WCDMA, GSM, UMTS, CDMA 2000 cellular standards. This included:

- Spur reduced PLL charge pump
- GSM gain, noise & linearity analysis
- Enhanced linearity LNA biasing
- Active RC filters and gmC filters
- WCDMA analog base-band
- Delta-Sigma ADC for CDMA 2000
- Auto-compensated process circuits
- New foundry processes: RF-CMOS & SiGe

July 1998 – September 2000: **Fairchild Semiconductor,** San Diego, California
Mixed signal IC design: designer and technical mentor for the department. Designs included:

- ADC's,14, 8 bit, VCO/counter & pipeline
- DAC, 10 bit, 300 MHz, I-steering
- Thermal cooling monitor/control IC
- LDO micro-power, 35 uA, for cellular
- PLL, 300MHz, for clock recovery
- Product demonstration/test PCB design
- Li-ion battery protection & charger IC
- Power systems, batteries & chargers

February 1996 - June 1998: **LSI Logic - Mixed Signal Design Group,** Milpitas, California
CMOS Mixed Signal IC Design: Done for a standard product cell library.
Designs included:

- PLL, 300MHz & 1GHz CDR & Freq. Synth.
- DVD timing recovery & controller
- DAC, 10 bit, current steering
- ADC's, 6 bit flash & 10 bit, sub-ranging
- CMOS foundry/process development
- Band-gap & Process calibration circuits

June 1994 - November 1995: **Quantum Corporation**, Milpitas, California

- Power Drive IC's and PCB design used for hard disk drives spindle and servo motors

October 1990 - March 1994: **EXAR Corporation**, San Jose, California

- HDD read channels, pre-amplifiers & LNA's
- Programmable gmC filters
- Clock and Data Recovery
- Frequency synthesizer PLL's

Academic & Professional:

- UCSD ECE graduate studies, Lecturer, winter quarter, 2010, ECE-264C, ADC and DAC IC Design
- Stanford University, invited speaker, Rethinking Analog Design - Simulation vs. Silicon, May 2010,
- Chairman 2005 - 2011 IEEE San Diego – Solid State Circuits, Microwave Theory and Techniques
- IEEE JSSC & IEEE MTT, Reviewer for submitted publications, 2003 - 2010
- UCSD Extension, Instructor, "CMOS Analog and Mixed Signal IC Design" 1999 - 2002
- Senior Member of IEEE, San Diego IEEE Executive Committee, Silicon Valley Consultants Group

Publications:

- "Marketing And Technology Collide In Competitive Chip Design" Electronic Design, 10/11/2012
- "Protect Your Fortress From ESD" Electronic Design, 8/9/2012
- "Academic Simplifications Produce Meaningless Equations" Electronic Design, 6/13/2012
- "Simple Grounding Rules Yield Huge Rewards" Electronic Design, 4/27/2012
- "Tiny Transistors! Giant Molecules! Moore's Law Crashes Into The Laws of Physics" ED, 4/9/2012
- "Efficient Simulation and Validation for Mixed-Signal SOCs" EDN Magazine, 3/29/2007
- "Determine Foundry-Model Problems Without Touching a Wafer" Chip Design Magazine April-May 2006
- "Simulation Vs. Silicon – Avoid Costly Mistakes With Accurate Models" Electronic Design, 10/28/2004
- "Signal Integrity Effects in Custom IC and ASIC Designs, multi-author, 2002, ISBN 0-471-15042-8
- "BiCMOS 5HPE A New Si-Ge Technology for HF & RF Apps." IBM Micro News, Vol. 7, No. 4, 2001
- "Designing Analog and Mixed Signal Circuits on Digital CMOS Processes" EDN, 8/3/2000
- "Noise Reduction Is Crucial to Mixed-Signal Design Success " Electronic Design, 10/30/2000, 12/4/2000

Patents:

- USPTO – 7,974,052: Method and Apparatus For Switched ESD Protection
- USPTO – 7,256,573: Distributed Active Transformer Power Control Techniques
- USPTO – 7,043,206: Fully Integrated Offset Compensation Feedback Circuit
- USPTO – 7,027,791: Analog Baseband Signal Processing and Method
- USPTO – 6,657,494: Variable Gain Mixer Amplifier With Fixed DC Operating Voltage Level

Design Tools:
Semiconductor – Cadence, Analog Artist, Spectre, Spectre-RF, Virtuosso-XL, OCEAN Scripts, SPICE, HSPICE Mentor Graphics, Design Architect, Accusim, Calibre, Viewlogic, Verilog-AMS, Verilog-A
PCB – Orcad, Altium Designer, Mentor-PADS **Electromagnetic -** ASITIC, Sonnet **System & Lab –** Matlab, Simulink, Agilent ADS, LabView **Digital –** Verilog, Xilinx ISE design suite, Atmel Studio IDE.

Education: MSEE & BSEE - Worcester Polytechnic Institute, Worcester MA